REMARKS

Claims 1-4 were examined. The Examiner rejects claim 1 under 35 U.S.C. § 112, first paragraph as containing subject matter which was allegedly not described in the specification in such a way as to enable one skilled in the art to make or use the invention.

In addition, the Examiner rejects claims 1-3 under 35 U.S.C. § 103(a) as being unpatentable over U. S. Patent 5,274,568 to Blinne et al (hereinafter "Blinne") in view of U.S. Patent 4,698,760 to Lembach et al (hereinafter "Lembach"). The Examiner also rejects claim 4 as being unpatentable over Blinne in view of Lembach and the article "An Accurate and Efficient Multiple Delay Simulator for MOS Logic Circuits Using Polynomial Approximation," by Jun et al (hereinafter "Jun").

I. Formal Matters

Applicant thanks the Examiner for citing the references listed on form PTO-892.

The Draftsperson has objected to the Figure 1 of the drawings because the margin on the right side is too small. Applicant submits a corrected drawing to overcome this objection.

Applicant also thanks the Examiner for acknowledging the claim for foreign priority under 35 U.S.C. § 119, and for confirming the receipt of papers filed in support of priority.

The Examiner objects to portions of the specification. Applicant amends the specification to correct minor typographical errors, and respectfully requests the Examiner to withdraw this objection accordingly.

Applicant respectfully traverses the rejections of claims 1-4 as follows.

II. Rejection of Claim 1 under 35 U.S.C. § 112, first paragraph.

Applicant amends the claims to correct minor typographical and grammatical errors, and to more broadly recite the features of Applicant's invention. These amendments are also there for precision of language and, as noted, do not narrow the scope of the original claims.

The Examiner rejects claim 1 under 35 U.S.C. § 112, first paragraph as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to make or use the invention.

Applicant respectfully disagrees. In particular, the specification describes the delay analysis system of claim 1 as having a library that "contains information on the delay time of each combination of input pins...and output pin" (page 6, lines 1-3). In addition, the specification discloses that "the present invention...uses a truth table (table showing the correspondence between input logical values and output logical values) such as the one shown in FIG. 1(c)" (page 6, lines 19-22). Figure 1(c) depicts the truth table for an AND gate, which is the example used in the specification.

Furthermore, the specification explains that the operation of the logic circuit "is shown also in FIG. 3 using the timing waveforms and the inputs having the change points to be considered when calculating the delay time" (page 7, lines 2-5). Figure 3 combines the truth table of figure 1(c) with the rise and fall information for each input of Figure 1(b) to show that based on the logic operation of the circuit, a different input is used when calculating the delay

time of the circuit. In the delay analysis of the AND gate described in the specification, only the delay time on the input which falls first is needed to calculate the delay time of the output, because in an AND gate, if any one of the inputs falls, the output falls.

As is noted in the specification, the conventional delay analysis library, in which no logic value table is used, calculates excessively long delay times for the logic circuit, because it uses the delay time of the inputs which falls last regardless of the particular logic operation of the circuit. The conventional delay analysis system uses the logic operation of the circuit to identify the instances where the delay time for the circuit can be determined based on only one input signal rather than two (page 2, lines 8-16).

Accordingly, claim 1 is enabled by Applicant's original specification, and the Examiner's §112, first paragraph, rejection should be withdrawn.

III. Rejection of Claims 1-4 under 35 U.S.C. § 103(a)

The Examiner rejects claims 1-4 under 35 U.S.C. § 103(a) as being unpatentable over Blinne in view of Lembach.

The Examiner indicates that Lembach discloses circuits that perform various predesigned logical combinations on the basis of the signals detected at the input terminals of the circuit. However, this disclosure is merely the definition of a logic circuit. In fact, as the Examiner states, neither Lembach nor Blinne teach or suggest storing the logical information of the circuit in the delay time library. Nothing in Blinne or Lembach teaches or suggests using the particular logic characteristics of each logic circuit in the delay analysis.

The Examiner contends that it would have been obvious to one having ordinary skill in the art that it was not necessary to store the logic information in the delay time information tables in the library, because in Lembach "the circuits automatically detected the signals and performed the logic operation on the basis of those signals" and because "the delay times computed by Blinne had taken into account the logical operations involved."

Applicant respectfully disagrees.

Lembach and Blinne perform their circuit analysis by treating the inputs of each logic circuit independently, but in practice, logic circuits operate by treating the inputs jointly. By measuring the delay times of the inputs independently of each other, the delay time analysis systems of Lembach and Blinne will record a maximum delay time for the logic circuit that is longer than what will be found in practice.

Specifically, in analyzing the delay times for logic circuits, Lembach treats each logic circuit as if it has only one input and one output (Lembach, column 5, lines 45-50). If, for example, the logic circuit being analyzed is a two input AND gate, analyzing the delay times for each input independently will lead the analysis to record the circuit's maximum delay time for a falling output (i.e. a logic value of 0) as the **longer** of the delay times measured for each input signal. While this system would produce the correct delay time for an OR gate, where the output falls after all inputs have fallen, in an AND gate this delay time is too long. In an AND gate, the output falls as soon as the input with the shortest delay time falls, because the signal levels for the other inputs are not needed to determine the output.

Similarly, Blinne ignores the logic operation of the circuit by also recording each of the many inputs of a logic circuit independently. In Blinne, the method used is to fix the inputs not being measured to a predetermined logic level while measuring the delay time of the remaining input (Blinne, Fig. 1 and column 8, lines 33-39). In calculating the maximum delay time for the circuit using this method, Blinne will use the delay time of the input with the **longest** delay time. This delay time is longer than what would be found in normal operation in an AND gate, for example, because in that case the output falls as soon as the input with the shortest delay time falls.

If the logic operation of the circuit is considered during the delay analysis, as defined in claims 1-4, then the **shorter** of the delay times for the falling of the two inputs will be recorded, which more accurately reflects the actual delay times of the circuit.

Therefore, it would not have been obvious for a person of ordinary skill in the art to use the delay time analysis systems of Lembach or Blinne to measure the delay time of a logic circuit by considering its logic operation as required by Applicant's claims 1-4.

In view of the foregoing, the application is believed to be in condition for allowance, and such action is hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, he is kindly requested to contact the undersigned attorney at the telephone number listed below.

Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee, except for the Issue Fee, for such extension is to be charged to Deposit Account No. 19-4880.

Respectfully submitted,

Howard L. Bernstein
Registration No. 25,665

SUGHRUE MION, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3213
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

Date: January 14, 2002

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The specification should be changed as follows:

On page 6, replace the paragraph beginning "The table shown..." at line 4 with:

"The table shown in FIG. 1(b) represents delay times for the combinations of an input pin and an output pin as they rise or fall. For example, on the first line, the delay time of 1 ns means that the delay between the time the signal at the input pin (terminal 1) of a 2-input AND element goes from low to high (rises) and the time the signal at the output pin (terminal 3) goes from low to high (rises) is 1 ns. Similarly, on the fifth line, the delay time of ~~2~~ 5 ns means that the delay between the time the signal at the input pin (terminal ~~1~~2) of a 2-input AND element goes from low to high (rises) and the time the signal at the output pin (terminal 3) goes from low to high (~~falls~~rises) is 5 ns. Note that delay time information on the rise and fall of input and output pins, such as that shown in FIG. 1(b), is contained also in the conventional delay analysis library."

IN THE CLAIMS:

The claims are amended as follows:

1. A delay analysis system for making a delay analysis of a logic circuit,

said system having a delay analysis library containing connection information on a plurality of circuits and delay time information on rises and falls of each input terminal and output terminal of said plurality of circuits,

wherein said library further contains logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of said plurality of circuits, and

wherein, when making a delay analysis of the logic circuit including at least one of said plurality of circuits, a delay time ~~between the input terminal and the output terminal~~ is selected from said delay time information~~,~~ according to a logic~~al~~ operation of said ~~at least one of~~ circuit~~s~~, ~~from the delay time information on the rises and falls of the input and output terminals of said plurality of circuits for use in delay calculation, said logical operation being specified by said logical operation information, said delay time information being stored in said library, and delay calculation is performed~~.

2. A delay analysis system for making a delay analysis of a logic circuit, said system having a delay analysis library containing connection information on a plurality of circuits and delay time information on rises and falls of each input terminal and output terminal of said plurality of circuits,

wherein said library further contains logical operation information representing correspondence between a logical value of each input terminal and ~~the~~ a logical value of the output terminal of at least one of said plurality of circuits, and

wherein, when making a delay analysis of ~~the~~ a logic circuit, a delay time between the input terminal and the output terminal is selected from said delay time information~~,~~ according to a logic~~al~~ operation of said circuits, ~~from the delay time information on the rises and falls of the~~

~~input and output terminals of said plurality of circuits for use in delay calculation, said logical operation being specified by said logical operation information, said delay time information being stored in said library, and delay calculation is performed.~~

3. A method for making a delay analysis of a logic circuit, comprising the steps of:

referencing ~~as library information~~ a delay analysis library containing connection information on a plurality of circuits, delay time information on rises and falls of each input terminal and output terminal of at least one of said plurality of circuits, and logic operation information representing correspondence between a logical value of each input terminal and ~~the~~ a logical value of the output terminal of at least one of said plurality of circuits; and

selecting the delay time ~~between the input terminal and the output terminal~~ of at least one of said ~~plurality of~~ circuits from said delay time information ~~included in the logic circuit as the delay time during the rise or fall of the output terminal of said at least of circuits, according to a logical operation of said at least one of circuits, from the delay time information on the rise and fall of each input terminal and the output terminal of said plurality of circuits,~~ according to ~~said~~ a specified logical ~~operation~~ operation of said circuit ~~being specified by said logical operation information, said delay time information being stored in said library, to perform delay calculation~~.

4. A computer-readable medium having stored thereon a program for executing:

(a) a process step comprising

~~(a1)~~ referencing ~~as library information~~ a delay analysis library containing connection information on a plurality of circuits, delay time information on rises and falls of each input terminal and output terminal of each one of said plurality of circuits, and logic operation information representing correspondence between a logical value of each input terminal and ~~the~~ a logical value of the output terminal of each one of said plurality of circuits; and

~~(a2)~~ selecting the delay time ~~between the input terminal and the output terminal~~ of at least one of said ~~plurality of~~ circuits from said delay time information ~~included in the logic circuit as a delay time during the rise or fall of the output terminal of said at least of circuits,~~ according to a logic~~al~~ operation of said ~~at least one of~~ circuit~~s, from the delay time information on the rise and fall of each input terminal and the output terminal of said plurality of circuits, said logical operation being specified by said logical operation information, said delay time information being stored in said library~~; and

(b) a process step of performing a delay calculation ~~with~~ using said selected delay time as a propagation delay time of said at least one of circuits.